CS211 Digital System and Lab

Spring 2012

Lectures	T: 16:30 ~ 17:45, R:16:30 ~ 17:45
Classroom	ITC building (N1) 111(lecture), ITC building (N1) 201(experiments)
Course Web Page	KLMS on KAIST Portal
Instructor	Prof. Soontae Kim (김순태)
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Office Hour	after class or via appointment

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Objective of the Course

This course is intended for an introductory course in digital logic design. It will teach students fundamental concepts in classical manual digital design and illustrate clearly the way in which digital circuits are designed today.

Prerequisites Basic math, basic electronics, preferably discrete mathematics

Textbook

Fundamentals of Digital Logic with VHDL Design, 3rd ed., McGRAW HILL International Edition, 2009.

Grading Policy

Six homework assignments	20%
Midterm	25%
Final	25%
Lab	25%
Attendance	5% (-1 on missing an attendance, two late attendances are equal to one miss attendance)

Cheating is **not allowed** in any of exams and homework assignments. You will be given **zero** points for cheating. Show your own efforts.

Late homework submission will be given 50% points by next day of the deadline, after which no point will be given.

Do not move around and **do not make noises** during class hours. You will be asked to leave classroom for these cases.

Sleeping is not allowed in class hours. Please leave the classroom when you are too sleepy and I will not count it as an attendance miss.

Course Schedule (subject to change)

Week	Date	Topic	Reading (textbook)	Assignments
1	3/5	Introduction & chapter 1	Ch. 1	
	3/7	Logic gates and networks, and Boolean algebra	Ch. 2.1~2.5	
2	3/12	Synthesis, logic networks, and examples	Ch. 2.6 ~ 2.8	
	3/14	Switches, gates, and standard chips	Ch. 3.1 ~ 3.5	HW#1
3	3/19	No class (travel to attend DATE conference)		
	3/21	No class (travel to attend DATE conference)		
4	3/26	Programmable logic devices, standard cells, gate arrays, and MOSFET	Ch. 3.5 ~ 3.8.4	
	3/28	Practical aspects, transmission gates, and PLDs	Ch. 3.8.5 ~ 3.10	
5	4/2	Karnaugh Map, minimization, and multi-level circuits,	Ch 4.1 ~ 4.5	HW#2
	4/4	Multi-level synthesis and multi-level circuits	Ch. 4.6 ~ 4.7	
6	4/9	Tabular method and cubical technique for minimization	Ch 4.8 ~ 4.11	
	4/11	Number representations, addition, and signed numbers	Ch. 5.1 ~ 5.3	
7	4/16	Fast adders, multiplication, and other number representations	Ch. 5.4 ~ 5.7	HW#3
	4/18	Multiplexers, decoders, encoders, etc	Ch. 6.1 ~ 6.5	
8	4/23	midterm	16:00~18:00	
	4/25	No class		
9	4/30	Latches	Ch 7.1 ~ 7.3	
	5/2	Flip flops and registers	Ch. 7.4 ~ 7.8	
10	5/7	Counters and reset synchronization	Ch. 7.9 ~ 7.11	HW#4
	5/9	Basic design, state assignment and Mealy state model	Ch 8.1 ~ 8.3	
11	5/14	Serial adder and state minimization	Ch. 8.5 ~ 8.6	
	5/16	Design of counter and FSM	Ch. 8.7 ~ 8.8	
12	5/21	Analysis, algorithmic state machine, and formal model	Ch. 8.9 ~ 8.11	HW#5
	5/23	Analysis and synthesis of asynchronous circuits	Ch. 9.1 ~ 9.3	
13	5/28	State reduction	Ch. 9.4	
	5/30	State assignment	Ch. 9.5	
14	6/4	Hazards and example	Ch. 9.6 ~ 9.7	HW#6
	6/6	holiday		
15	6/11	Building block circuits and clock synchronization	Ch. 10.1, 10.3	
	6/13	Reserved		
16	6/18	Final exam		
	6/20	Final exam		