ICE0502: Computer Architecture (Summer 2008)

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Classroom: L405
Class hours: M/W 13:00 ~ 16:00

Course description: The class will review fundamental structures in modern microprocessor and computer system architecture design. Tentative topics will include performance metric, instruction set design, memory system design, pipelining, and other techniques to exploit instructional-level parallelism. We will also cover basics of multiprocessor systems and thread-level parallelism.

Prerequisite: undergraduate computer architecture course, “Computer Organization & Design” by Patterson and Hennessy is preferred as the text of your undergraduate course

Textbook: Computer Architecture: A Quantitative Approach, 3rd Edition, John L. Hennessy and David A. Patterson, Morgan Kaufmann Publishers

Tentative Schedule (out-of-order):
• Review – performance, pipelining, and memory hierarchy (2 lectures)
• Instruction level parallelism (5 lectures))
• Limits on ILP (1 lecture)
• Multi-processors and thread-level parallelism (2 lectures)
• Memory system (2 lectures)
• Low-power and reliability issues (1 lecture)
• Final project presentations (1 lecture)

Grading (tentative):

Exam1:	20% (July 9, Wednesday)
Exam2	20% (August 4, Monday)
Homework:	10%
Project:	40%
Attendance	10%

* Exams: in-class closed book
* Late homework will receive zero point
* Copied homework will receive zero point
* You will receive zero point in exams & homework assignments for cheating

Available tools for course term projects

- Simplescalar
- EXTREM
- SimplePower
- Wattch
- ISE/Modelsim
- etc