# CS311: Computer Organization

Spring 2010

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| **Lectures** | T/R 10:30 ~ 11:45AM |
| **Classroom** | EECS#1220(제 2 공동강의실) |
| **Course Web Page** | **http://ecl.kaist.ac.kr/xe/?mid=course_cs311** |
| **Instructor** | Prof. Soontae Kim (김순태) |
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| Office Hour | W 1:00 ~ 3:00PM, or via appointment, email, and phone |

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**Objective of the Course**

We will study the internals of modern computer systems and how to design them. We will first look at instruction set design issues. Then, we will design the datapath and memory system. Peripheral devices are also studied. After taking this course, you should be able to understand the organization and design issues of computer systems.

**Prerequisites**

Logic design(mendatory), experience with high-level language(C/C++) programming, basic math

**Textbook**

Patterson and Hennessy, Computer Organization and Design The hardware/software Interface, 4th Ed., Morgan Kaufmann Publishers, 2009.

**Grading Policy**

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| Homework assignments | 30% |
| Midterm exam | 30% |
| Final exam | 30%. |
| Attendance | 10% (-1 for missing a class) |

**Cheating Policy**

Cheating is **not allowed** in all exams and homework assignments. **You will be given zero points for cheating. Do not look at the solutions you obtained on the Internet for homework assignments.**

## Course Schedule (subject to change)

| Week | Date | Topic | Reading (textbook) | Assignments |
|---|---|---|---|---|
| 1 | 2/2 | Computer abstractions and Technology | Chapter1 | |
| | 2/4 | Instruction set architecture(ISA) | Chapter 2.1 ~2.3 | |
| 2 | 2/9 | ISA II | Chapter 2.4 ~2.7 | |
| | 2/11 | MIPS ISA | Chapter 2.8 ~2.10 | Hw#1 |
| 3 | 2/16 | No class | | KAIST birthday |
| | 2/18 | MIPS assembly programming | Section 2.11 ~ 2.13 | |
| 4 | 2/23 | MIPS assembling and compiling | Section 2.14 ~ 2.17 | |
| | 2/25 | Review - combinational logic | Appendix C | |
| 5 | 3/2 | Integer arithmetic | Section 3.1 ~ 3.4 | Hw#2 |
| | 3/4 | Floating-point arithmetic | Section 3.5 | |
| 6 | 3/9 | Performance | Chapter 1.4 | |
| | 3/11 | Review - sequential logic | Appendix C | |
| 7 | 3/16 | Building a datapath | Section 4.1 ~ 4.3 | Hw#3 |
| | 3/18 | Datapath – simple implementation | Section 4.4 | |
| 8 | 3/23 | Midterm exam | Chapter 1 ~ 4.4, Appendix C | |
| | 3/25 | Midterm exam | Chapter 1 ~ 4.4, Appendix C | |
| 9 | 3/30 | Pipelining - overview | Section 4.5 | |
| | 4/1 | Pipelining – datapath & control | Section 4.6 | Hw#4 |
| 10 | 4/6 | Pipelining – data hazards | Section 4.7 | |
| | 4/8 | Pipelining – control hazards and exceptions | Section 4.8 ~ 4.9 | |
| 11 | 4/13 | Instruction-level parallelism | Section 4.10 | |
| | 4/15 | Memory hierarchy – basics | Section 5.1, 5.2 | |
| 12 | 4/20 | Memory hierarchy – cache performance | Section 5.3 | Hw#5 |
| | 4/22 | Memory hierarchy – cache performance II | Section 5.3 | |
| 13 | 4/27 | Memory hierarchy – virtual memory | Section 5.4 | |
| | 4/29 | Memory hierarchy – virtual memory II | Section 5.4, 5.5 | |
| 14 | 5/4 | Disk & bus | Section 6.1 ~ 6.4 | |
| | 5/6 | Interface – interrupt & DMA | Section 6.4 ~ 6.8 | Hw#6 |
| 15 | 5/11 | Multicore & multiprocessors | Chapter 7 | |
| | 5/13 | Wrap-up or for buffering | | |
| 16 | 5/18 | Final exam | Chapter 4~7 | |
| | 5/20 | Final exam | Chapter 4~7 | |