CS311: Computer Organization

Fall 2011

Lectures	T/R 16:00 ~ 17:15PM
Classroom	EECS#2112 (제 2 강의실)
Course Web Page	**http://ecl.kaist.ac.kr/?mid=course_cs311**
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Objective of the Course

We will study the internals of modern computer systems and how to design them. We will first look at instruction set design issues. Then, we will design the datapath and memory system. Peripheral devices are also studied. After taking this course, you should be able to understand the organization and design issues of computer systems.

Prerequisites

Logic design (mendatory), experience with high-level language(C/C++) programming, basic math

Textbook

Patterson and Hennessy, Computer Organization and Design The hardware/software Interface, 4th Ed., Morgan Kaufmann Publishers, 2009.

Grading Policy

Homework assignments	30%
Midterm exam	30%
Final exam	30%
Attendance	10% (-1 for missing a class)

Cheating Policy

Cheating is **not allowed** in all exams and homework assignments. **You will be given zero points for cheating. Do not look at the solutions you obtained on the Internet for homework assignments.**

Course Schedule (subject to change)

Week	Date	Topic	Reading (textbook)	Assignments
1	9/1	Class introduction		
	9/6	Computer abstractions and Performance	Chapter1	
2	9/8	Instruction set architecture(ISA)	Chapter 2.1 ~2.3	
	9/13	Chooseok		Holiday
3	9/15	MIPS ISA	Chapter 2.4 ~2.7	Hw#1
	9/20	MIPS ISA II	Chapter 2.8 ~2.10	
4	9/22	MIPS assembly programming	Section 2.11 ~ 2.13	
	9/27	Review - combinational logic	Appendix C	
5	9/29	Integer arithmetic	Section 3.1 ~ 3.4	Hw#2
	10/4	Floating-point arithmetic	Section 3.5	
6	10/6	Review - sequential logic	Appendix C	
	10/11	Travel to ESWEEK		No class
7	10/13	Building a datapath	Section 4.1 ~ 4.3	Hw#3
	10/18	Datapath – simple implementation	Section 4.4	
8	10/20	Midterm exam	Chapter 1 ~ 4.4, Appendix C	
	20/25	Midterm exam	Chapter 1 ~ 4.4, Appendix C	
9	20/27	Pipelining - overview	Section 4.5	
	11/1	Pipelining – datapath & control	Section 4.6	Hw#4
10	11/3	Pipelining – data hazards	Section 4.7	
	11/8	Pipelining – control hazards	Section 4.8 ~ 4.9	
11	11/10	Pipelining – exceptions		
	11/15	Instruction-level parallelism	Section 4.10	Hw#5
12	11/17	Memory hierarchy – basics	Section 5.1, 5.2	
	11/22	Memory hierarchy – cache performance	Section 5.3	
13	11/24	Memory hierarchy – cache performance II	Section 5.3	
	11/29	Memory hierarchy – virtual memory	Section 5.4	Hw#6
14	12/1	Memory hierarchy – virtual memory II	Section 5.4, 5.5	
	12/6	Travel to Micro		No class
15	12/8	Disk, bus, interrupt & DMA	Section 6.1 ~ 6.8	
	12/13	Multicore & multiprocessors	Chapter 7	
16	12/15	Final exam	Chapter 4~7	
	12/20	Final exam	Chapter 4~7	