

# Special Topics on Low-Power Computing

**Course Description:** This course studies low-power issues at various levels of computer systems.

- Fundamentals of low-power computing
- Low-power architecture
- Low-power OS issues
- Compiler-based low-power computing
- Voltage scaling
- Low-power DRAMs
- Low-power caches
- Low-power displays
- Low-power wireless communication
- Interplay of low-power and reliability

Throughout the course, students will be asked to apply their understanding of the above topics on exam and term project. Any graduate students are welcome to this class. You will better understand computer systems and power issues. You can work at any level including architecture, OS, compiler, application, algorithm, etc.

**Prerequisites:** undergraduate operating systems, computer architecture

**Textbook:** no textbook. Recent papers and lecture notes will be used.

Instructor: Prof. **Soontae Kim**  
Phone: (042) 350-3554 (office)  
Email: kims@kaist.ac.kr  
Web: <http://ecl.kaist.ac.kr>

TA: Jongmin Lee  
Email: square55@kaist.ac.kr  
Phone: (042)-350-7854

**Grading Policy:** Final grade will consist of the followings:

Exam 30%  
Attendance & participation 15%  
Three presentations 15%  
Two intermediate reports 10%  
Term paper 30%

Course Schedule (subject to change)

Week	Date	Topic	talk	Assignments
1	9/2	Introduction	professor	
	9/7	Power/Energy#1	Professor	
2	9/9	Power/Energy#2	Professor	
	9/14	Power/Energy#3	Professor	
3	9/16	Power/Energy#4	Professor	
	9/21	No class		Chuseok
4	9/23	No class		Chuseok
	9/28	Proposal presentation	Students	Prepare 10 min proposal presentation
5	9/30	Presentation#1	Students	Prepare 1 hour presentation for 1 <sup>st</sup> paper
	10/5	No class		Attend international conference
6	10/7	No class		Attend international conference
	10/12	Presentation#2	Students	Prepare 1 hour presentation for 1 <sup>st</sup> paper
7	10/14	Presentation#3	Students	Prepare 1 hour presentation for 1 <sup>st</sup> paper
	10/19	Presentation#4	Students	Prepare 1 hour presentation for 1 <sup>st</sup> paper
8	10/21	Presentation#5	Students	Prepare 1 hour presentation for 1 <sup>st</sup> paper
	10/26	Presentation#6	Students	Prepare 1 hour presentation for 1 <sup>st</sup> paper
9	10/21	Presentation#7	Students	Prepare 1 hour presentation for 1 <sup>st</sup> paper
	10/26	No class		Exam preparation
10	10/28	exam		
	11/2	Progress presentation#1	Students	Prepare 10 min presentation for progress
11	11/4	Progress presentation#2	Students	Prepare 10 min presentation for progress
	11/9	Presentation#8	Students	Prepare 1 hour presentation for 2 <sup>nd</sup> paper
12	11/11	Presentation#9	Students	Prepare 1 hour presentation for 2 <sup>nd</sup> paper
	11/16	Presentation#10	Students	Prepare 1 hour presentation for 2 <sup>nd</sup> paper
13	11/18	Presentation#11	Students	Prepare 1 hour presentation for 2 <sup>nd</sup> paper
	11/23	Presentation#12	Students	Prepare 1 hour presentation for 2 <sup>nd</sup> paper
14	11/25	Presentation#13	Students	Prepare 1 hour presentation for 2 <sup>nd</sup> paper
	11/30	Presentation#14	Students	Prepare 1 hour presentation for 2 <sup>nd</sup> paper
15	12/9	Final presentation#1	Students	Prepare 15 min presentation for whole project
	12/14	Final presentation#2	Students	Prepare 15 min presentation for whole project

## List of papers for your projects

### Voltage scaling & system-wide power reduction

1. **Real-Time Dynamic Voltage Scaling for Low-Power Embedded Operating systems, SOSOP, 2001.**
2. **Into the Wild: Studying Real User Activity Patterns to Guide Power Optimizations for Mobile Architectures, Micro 2009.**
3. ***CoolSpots*: Reducing the Power Consumption of Wireless Mobile Devices with Multiple Radio Interfaces, MobiSys 2006.**

### DRAM power

4. **Improving SDRAM Access Energy Efficiency for low-power embedded systems, TECS 2008.**
5. **The Virtual Write Queue: Coordinating DRAM and Last-Level Cache Policies, ISCA 2010.**
6. **Power-Efficient DRAM Speculation, HPCA 2008.**
7. **A Durable and Energy Efficient Main Memory Using Phase Change Memory Technology, ISCA 2009.**

### Caches & RF

8. **Hybrid Cache Architecture with Disparate Memory Technologies, ISCA 2009.**
9. **Bank-aware Dynamic Cache Partitioning for Multicore Architectures, ICCP 2009.**
10. **Row/Column Redundancy to Reduce SRAM Leakage in Presence of Random Within-Die Delay Variation, ISLPED 2008.**
11. **Processor Reliability Enhancement through Compiler-Directed Register File Peak Temperature Reduction, DSN 2009.**

### Display power

12. **Smart driver for power reduction in next generation bistable electrophoretic display technology, Codes/ISSS 2007.**  
**System-Level Display Power Reduction Technologies for Portable Computing and Communications Devices, Portable 2007.**
13. **Transient Fault Prediction Based on Anomalies in Processor Events, DATE 2007.**