ICE1220: Computer Architecture

Fall 2008

Lectures	T/R 9:00 ~ 10:15AM
Classroom	
Course Web Page	on cyber ICU

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Objective of the Course

We will study the internals of modern computers and how to design them. We will first look at instruction set design issues. Then, we will design datapath and memory system. Peripheral devices are also studied. After taking this course, you should be able to understand the organization and design issues of modern computer systems.

Prerequisites

Logic design(mendatory), experience with high-level language(C/C++) programming

Textbook

Patterson and Hennessy, Computer Organization and Design The hardware/software Interface, 3rd international ed., Morgan Kaufmann Publishers, 2005.

Grading Policy

Homework assignments	30%
Midterm exam	30%
Final exam	35%.
Attendance	5% (-1 for a miss)

Cheating Policy

Cheating is **not allowed** in exams and homework assignments. **You will be given zero points for cheating. Do not look at the solutions you obtained on the Internet for homework assignments**

Course Schedule (subject to change)

Week	Date	Topic	Reading (textbook)	Assignments
1	8/26	Computer abstractions and Technology	Chapter1	
	8/28	Instruction set architecture(ISA)	Chapter 2	
2	9/2	ISA II	Chapter 2	
	9/4	MIPS ISA	Chapter 2	Hw#1
3	9/9	MIPS instructions	Section 2.1 ~ 2.5	
	9/11	MIPS assembly programming	Section 2.6 ~ 2.9	
4	9/16	MIPS assembling and compiling	Section 2.10 ~ 2.15	Hw#2
	9/18	Review - combinational logic	Appendix B	
5	9/23	Review - sequential logic	Appendix B	
	9/25	Integer arithmetic	Section 3.1 ~ 3.5	
6	9/30	Floating-point arithmetic	Section 3.6	Hw#3
	10/2	Performance	Chapter 4	
7	10/7	Recess		
	10/9	Recess		
8	10/14	midterm	Chapter 1 ~ 4, Appendix B	
	10/16	midterm	Chapter 1 ~ 4, Appendix B	
9	10/21	Building a datapath	Section 5.1 ~ 5.3	
	10/23	Datapath – single cycle implementation	Section 5.4	
10	10/28	Datapath – multicycle implementation	Section 5.5	
	10/30	Datapath – multicycle implementation and exceptions	Section 5.5, 5.6	Hw#4
11	11/4	Pipelining - overview	Section 6.1	
	11/6	Pipelining - datapath	Section 6.2, 6.3	
12	11/11	Pipelining – data hazards	Section 6.4, 6.5	
	11/13	Pipelining – branch hazards and exceptions	Section 6.6, 6.8	Hw#5
13	11/18	Memory hierarchy – basics	Section 7.1, 7.2	
	11/20	Memory hierarchy – cache performance	Section 7.3	
14	11/25	Memory hierarchy – virtual memory	Section 7.4	
	11/27	Memory hierarchy – virtual memory & framework	Section 7.4, 7.5	Hw#6
15	12/2	Disk & bus	Section 8.1 ~ 8.4	
	12/4	Interface – interrupt & DMA	Section 8.4 ~ 8.8	
16	12/9	Final exam	Chapter 5 ~ 8	
	12/11	Final exam	Chapter 5 ~ 8	