CS311: Computer Organization

Fall 2014

Classroom	N1 Building Room 102
Course Web Page	**http://ecl.kaist.ac.kr/?mid=course_2014_fall_cs311 or LIMS**
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Office Hour	W/F 9:30~ 11:30

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Objective of the Course

We will study the internals of modern computer systems and how to design them. We will first look at instruction set design issues. Then, we will design the datapath and memory system. Parallel processors are also studied. After taking this course, you should be able to understand the organization and design issues of modern computer systems and to explain them to other non-major people.

Prerequisites

Logic design (mendatory), experience with high-level language(C/C++) programming, basic math

Textbook

Patterson and Hennessy, Computer Organization and Design The hardware/Software Interface, 5th Ed., Elsevier Korea LLC (Asian edition).

Grading Policy (tentative)

Homework assignments	20%
Project	20%
Midterm exam	25%
Final exam	30%
Attendance	5% (-1 for missing a class)

Cheating is **not allowed** in all exams and homework assignments. **You will be given zero points for cheating. Do not look at the solutions you obtained on the Internet for homework assignments.**

Do not make noise and move around not to annoy me and other students. If you do so, I may ask you to leave the classroom.

Course Schedule (subject to change)

Week	Date	Topic	Reading (textbook)	Assignments
1	9/3	Computer abstractions and technology	Chapter1	
	9/5	Instruction set architecture(ISA)	Chapter 2.1 ~2.3	
2	9/10	No class		Holiday
	9/12	MIPS ISA	Chapter 2.4 ~2.7	
3	9/17	MIPS ISA II	Chapter 2.8 ~2.10	
	9/19	MIPS assembly programming	Section 2.11 ~ 2.13	Hw#1
4	9/24	Review - combinational logic	Appendix ?	
	9/26	Integer arithmetic	Section 3.1 ~ 3.4	
5	10/1	Floating-point arithmetic	Section 3.5	
	10/3	No class		Holiday
6	10/8	Review - sequential logic	Appendix C	
	10/10	Building a datapath	Section 4.1 ~ 4.3	Hw#2
7	10/15	Datapath – simple implementation	Section 4.4	
	10/17	Pipelining - overview	Section 4.5	
8	10/20	Midterm exam	Chapter 1 ~ 4.5, Appendix ?	
9	10/29	Pipelining – datapath & control	Section 4.6	
	10/31	Pipelining – data hazards	Section 4.7	
10	11/5	Pipelining – control hazards	Section 4.8	
	11/7	Pipelining – exceptions	Section 4.9	
11	11/12	Instruction-level parallelism	Section 4.10	Hw#3
	11/14	Memory hierarchy – basics	Section 5.1, 5.2	
12	11/19	Memory hierarchy – cache performance	Section 5.3	
	11/21	Memory hierarchy – cache performance II	Section 5.4	
13	11/26	Memory hierarchy – virtual memory	Section 5.5~5.7	
	11/28	Memory hierarchy – common framework	Section 5.8~5.10	
14	12/3	Memory hierarchy – real stuffs	Section 5.13	Hw#4
	12/5	Reserved		
15	12/10	Parallel processing, SIMD, multithreading	Section 6.1 ~ 6.4	
	12/12	Multicore & multiprocessors	Chapter 6.5 ~6.8	
16	12/15	Final exam	Chapter 4.6~6	