Computer Architecture Term Project Topic List

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I. Basic Information for Term Project

- ✓ You will get a term project proposal presentation one week later after midterm exam: April 30th (Tue.).
- ✓ You should select appropriate topics for your term project.
- ✓ Term project topics have to be related to computer architecture.
- ✓ The topic list below is just examples that you can do as a term project. So, you can select other topics as you want if you have better idea.
- ✓ References for each topics in the list are papers or documentations that help you to do the term project. You can get some helps on them, and it does not mean that you have to get similar results after the term project.

II. Term Project Topics

- ✓ Followings are term project topics that you can do.
- ✓ There are two major topics: 'Memory' and 'Non-Memory'.
- ✓ There are seven minor topics: 'DRAM', 'RCM', 'STT-MRAM', 'Flash memory and SSD', 'CPU', 'GPU', and 'Artificial Intelligence & Computer Architecture'.
- ✓ Each minor topics has several detailed topics, and each detailed topics has its own references.

1. Memory

A. DRAM

i. Low power dram design

- ➢ Memory controller scheduling for low power [1]
- ➢ Fine-grained activation [2]
- ➢ Refresh power reduction [3]

ii. High performance DRAM design

- ➢ Memory controller scheduling for high performance [4]
- ➢ DRAM compression [5]

iii. Quality of Service (QoS)

- ➢ Memory controller scheduling for fairness [6]

B. PCM (Phase Change Memory)

i. Device comparison

- ➢ DRAM and PCM performance comparison [1]

ii. Low power and high performance PCM design

- ➢ Architectures to reduce overhead from PCM [2]

iii. Reliability issues

- ➢ Hard fault failure minimization [3]

C. STT-MRAM (Spin Torque Transfer Magnetic RAM)

i. Device comparison

- ➢ Performance and power comparison between SOT and STT-MRAM [1, 2]

ii. Embedded memory

- STT-MRAM for mobile system [3]

iii. Reliability issues

- Failure and reliability analysis of STT-MRAM [4]

D. Flash memory and SSD

i. Garbage collection and wear leveling

- Garbage collection and wear leveling technique [1]

ii. SSD lifetime improvement

- Super-page management [2]

2. Non-Memory

A. CPU

i. Pipelining

- Deep pipelining performance comparison for ISAs [1]

ii. Parallelism

- Data level parallelism with Intel AVX instruction [2]

iii. Branch prediction

- High-performance, low-power branch predictor design [3]

B. GPU

i. SIMD utilization

- Thread level parallelism for higher SIMD utilization [1]

ii. Host-Device data copy optimization

- Host and device DRAM control with CUDA [2]

C. Artificial Intelligence & Computer Architecture

i. A.I.-support computer architecture

- Deep learning acceleration with GPU, NPU, and etc. [1, 2, 3]

ii. A.I-based computer architecture

- Neural network branch predictor [4]

III. References

- ✓ Followings are references for each detailed topics.
- ✓ You can refer them for your better term project results.

1. Memory

A. DRAM

[1] Fan, Xiaobo, Carla Schlatter Ellis, and Alvin R. Lebeck. "Memory controller policies for DRAM power management." ISLPED'01: Proceedings of the 2001 International Symposium on Low Power Electronics and Design (IEEE Cat. No. 01TH8581). IEEE, 2001.
[2] Zhang, Tao, et al. "Half-DRAM: a high-bandwidth and low-power DRAM architecture from the rethinking of fine-grained activation." 2014 ACM/IEEE 41st International Symposium on Computer Architecture (ISCA). IEEE, 2014.
[3] Liu, Jamie, et al. "RAIDR: Retention-aware intelligent DRAM refresh." ACM SIGARCH Computer Architecture News. Vol. 40. No. 3. IEEE Computer Society, 2012.
[4] Mutlu, Onur, and Thomas Moscibroda. "Parallelism-aware batch scheduling: Enhancing both performance and fairness of shared DRAM systems." ACM SIGARCH Computer Architecture News. Vol. 36. No. 3. IEEE Computer Society, 2008.
[5] Young, Vinson, Sanjay Kariyappa, and Moinuddin Qureshi. "Enabling Transparent Memory-Compression for Commodity Memory Systems." 2019 IEEE International Symposium on High Performance Computer Architecture (HPCA). IEEE, 2019.
[6] Mutlu, Thomas Moscibroda Onur. "Memory performance attacks: Denial of memory service in multi-core systems." USENIX security. 2007.

B. PCM (Phase Change Memory)

[1] Lee, Benjamin C., et al. "Architecting phase change memory as a scalable dram alternative." ACM SIGARCH Computer Architecture News 37.3 (2009): 2-13.
[2] Qureshi, Moinuddin K., Michele M. Franceschini, and Luis A. Lastras-Montano. "Improving read performance of phase change memories via write cancellation and write pausing." HPCA-16 2010 The Sixteenth International Symposium on High-Performance Computer Architecture. IEEE, 2010.
[3] Schechter, Stuart, et al. "Use ECP, not ECC, for hard failures in resistive memories." ACM SIGARCH Computer Architecture News. Vol. 38. No. 3. ACM, 2010.

C. STT-MRAM (Spin Torque Transfer Magnetic RAM)

[1] Prenat, Guillaume, et al. "Beyond STT-MRAM, spin orbit torque RAM SOT-MRAM for high speed and high reliability applications." Spintronics-based Computing. Springer, Cham, 2015. 145-157.
[2] Oboril, Fabian, et al. "Evaluation of hybrid memory technologies using SOT-MRAM for on-chip cache hierarchy." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 34.3 (2015): 367-380.
[3] Lee, Kangho, and Seung H. Kang. "Development of embedded STT-MRAM for mobile system-on-chips." IEEE Transactions on Magnetics 47.1 (2011): 131-136.
[4] Zhao, W. S., et al. "Failure and reliability analysis of STT-MRAM." Microelectronics Reliability 52.9-10 (2012): 1848-1852.

D. Flash memory and SSD

[1] Chang, Li-Pin. "On efficient wear leveling for large-scale flash-memory storage systems."

Proceedings of the 2007 ACM symposium on Applied computing. ACM, 2007.
[2] Kang, Mincheol, Wonyoung Lee, and Soontae Kim. "Subpage-Aware Solid State Drive for Improving Lifetime and Performance." IEEE Transactions on Computers 67.10 (2018): 1492-1505.

2. Non-Memory

A. CPU

[1] Clark, Douglas W. "Pipelining and performance in the VAX 8800 processor." ACM SIGARCH Computer Architecture News. Vol. 15. No. 5. IEEE Computer Society Press, 1987.
[2] Lomont, Chris. "Introduction to intel advanced vector extensions." Intel White Paper (2011): 1-21.
[3] Chang, Po-Yung, et al. "Branch classification: a new mechanism for improving branch predictor performance." International Journal of Parallel Programming 24.2 (1996): 133-158.

B. GPU

[1] Hong, Sunpyo, and Hyesoon Kim. "An analytical model for a GPU architecture with memory-level and thread-level parallelism awareness." ACM SIGARCH Computer Architecture News. Vol. 37. No. 3. ACM, 2009.
[2] Bader, Michael, et al. "Fast GPGPU data rearrangement kernels using CUDA." arXiv preprint arXiv:1011.3583 (2010).

C. Artificial Intelligence & Computer Architecture

[1] Rhu, Minsoo, et al. "vDNN: Virtualized deep neural networks for scalable, memory-efficient neural network design." The 49th Annual IEEE/ACM International Symposium on Microarchitecture. IEEE Press, 2016.
[2] Chen, Yu-Hsin, et al. "Eyeriss: An energy-efficient reconfigurable accelerator for deep convolutional neural networks." IEEE Journal of Solid-State Circuits 52.1 (2017): 127-138.
[3] Jouppi, Norman P., et al. "In-datacenter performance analysis of a tensor processing unit." 2017 ACM/IEEE 44th Annual International Symposium on Computer Architecture (ISCA). IEEE, 2017.
[4] Jiménez, Daniel A., and Calvin Lin. "Neural methods for dynamic branch prediction." ACM Transactions on Computer Systems (TOCS) 20.4 (2002): 369-397.