CS510: Computer Architecture

Instructor: Prof. Soontae Kim
Office : N1 903
Phone: (042) 350-3554
Email: kims@kaist.ac.kr
Course Web: Embedded Computing Lab at http://ecl.kaist.ac.kr
Office hours: right after class or via prior appointments

TA: Jinkwon Kim, Myoungjae Jang

Classroom: N1 Building Room # 111
Class hours: T/R 1:00 ~ 2:15PM

Course description: This class will review fundamental structures in modern microprocessor and computer architecture design. Topics include performance metric, memory system design, pipelining, exploiting instructional-level parallelism and its limits, multiprocessors, thread-level parallelism, and data-level parallelism.

Prerequisite: undergraduate computer architecture course, “Computer Organization & Design” by Patterson and Hennessy is preferred as the text of your undergraduate course. However, I will review pipelining and memory basics for you.

Textbook: Computer Architecture: A Quantitative Approach, 5th Edition, by John L. Hennessy and David A. Patterson, Morgan Kaufmann Publishers

Grading:

Midterm Exam:	25%
Final Exam:	20%
Attendance	5%
Homework:	20%

- Three homework assignments

Project: 30%

- Make a team of at most three students. You choose specific topics such as caches, memory, pipeline, ILP, DLP, TLP, GPU, power, reliability, security etc. and perform experiments using simulators and other tools. More details will be announced later.
- Two project presentations each 5%, final report 20%

Cheating: All forms of cheating are not allowed in this class. Examples include the followings.

- Do not copy solutions obtained from Internet, etc.
- Do not copy other students’ solutions. Discussion before solving problems is OK but you must not discuss about detailed solutions.
- Cheater will be given zero point and those who allow cheating will be given 50% of their earned points.

* Higher priority will be given to projects. If you select aggressive projects and show good implementation and experimental results, I will give you more points.

*Subject to change

Week	Date	Topic	Reading (textbook)	Assignments
1	2/26	Class introduction		
	2/28	Chapter1. Fundamentals of computer design	Ch1	
2	3/5	Chapter1. Fundamentals of computer design	Ch1	
	3/7	MIPS CPU design #1	Appendix A, undergraduate textbook	
3	3/12	MIPS CPU design #2	Appendix A, undergraduate textbook	
	3/14	Review-pipelining#1	Appendix C	
4	3/19	Review-pipelining#2	Appendix C	HW#1
	3/21	Instruction-level parallelism#1	Ch3	
5	3/26	Instruction-level parallelism#2	Ch3	
	3/28	Instruction-level parallelism#3	Ch3	
6	4/2	Instruction-level parallelism#4	Ch3	
	4/4	Limits of ILP#1	Ch3	
7	4/9	Review-caches#1	Appendix B	HW#2
	4/11	Review-caches#2	Appendix B	
8	4/16	Midterm exam		
	4/18	Midterm exam		
9	4/23	Proposal presentations		
	4/25	Advanced caches#1	Ch2	
10	4/30	Advanced caches#2	Ch2	
	5/2	Memory#1	Ch2	
11	5/7	Memory#2	Ch2	
	5/9	Vector architecture	Ch4	HW#3
12	5/14	GPU	Ch4	
	5/16	Multiprocessors#1	Ch5	
13	5/21	Multiprocessors#2	Ch5	
	5/23	Multiprocessors#3	Ch5	
14	5/28	Final project presentation#1		
	5/30	Final project presentation#2		
15	6/4	reserved		
	6/6	No class		holiday
16	6/11	Final exam		
	6/13	Final exam		Submit project reports