Computer Architecture Homework Assignment #3

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I. Submission and grading

- ✓ Due date: May, 17th (Tue.) 23:59:59.
- ✓ Submit your homework as a hardcopy into HW box prepared near the office room #922 in N1 building. Do not submit by KLMS or TA's e-mail.
- ✓ Late submissions will not be accepted. Please keep the submission due date.
- ✓ Each score has been written at the end of each question. The total score is 100.
- ✓ You will be given 0 point for any kind of cheating.
- ✓ Please explicitly denote number of each question and its answer. Otherwise, it can be considered as not be done.
- ✓ Please give detailed process how you solve questions. Otherwise, no point will be charged.

II. Questions

✓ Please solve every questions as below **(Total 100 points)**:

Q1. You are trying to appreciate how important the principle of locality is in justifying the use of a cache memory, so you experiment with a computer having an L1 data cache and a main memory (you exclusively focus on data accesses). The latencies (in CPU cycles) of the different kinds of accesses are as follows: cache hit, 1 cycle; cache miss, 105 cycles; main memory access with cache disabled, 100 cycles.

A. When you run a program with an overall miss rate of 5%, what will the average memory access time (in CPU cycles) be? **(10 points)**

B. Next, you run a program specifically designed to produce completely random data addresses with no locality. Toward that end, you use an array of size 256 MB (all of it fits in the main memory). Accesses to random elements of this array are continuously made (using a uniform random number generator to generate the elements indices). If your data cache size is 64 KB, what will the average memory access time be? **(10 points)**

C. If you compare the result obtained in part (B) with the main memory access time when the cache is disabled, what can you conclude about the role of the principle of locality in justifying the use of cache memory? **(13 points)**

D. You observed that a cache hit produces a gain of 99 cycles (1 cycle vs. 100), but it produces a loss of 5 cycles in the case of a miss (105 cycles vs. 100). In the general case, we can express these two quantities as G (gain) and L (loss). Using these two quantities (G and L), identify the lowest or minimum miss rate after which the cache use would be disadvantages. **(13 points)**

Q2. The LRU replacement policy is based on the assumption that if address A1 is accessed less recently than address A2 in the past, then A2 will be accessed again before A1 in the future. Hence, A2 is given priority over A1. Discuss how this assumption fails to hold when a loop larger than the instruction cache is being continuously executed. For example, consider a fully associative 128-byte instruction cache with a 4-byte block (every block can exactly hold one instruction). The cache uses an LRU replacement policy.

A. What is the asymptotic instruction miss rate for a 64-byte loop with a large number of iterations? **(10 points)**

B. Repeat part (A) for loop sizes 192 bytes and 320 bytes. **(10 points)**

C. If the cache replacement policy is changed to most recently used (MRU) (replace the most recently accessed cache line), which of the three above cases (64-, 192-, or 320-byte loops) would benefit from this policy? **(14 points)**

Q3. A program is running on a computer with a four-entry fully associative (micro) translation lookaside buffer (TLB):

VP#	PP#	Entry valid
5	30	1
7	1	0
10	10	1
15	25	1

The following is a trace of virtual page numbers accessed by a program. For each access indicate whether it produces a TLB hit/miss and, if it accesses the page table, whether it produces a page hit or fault. Put an X under the page table column if it is not accessed. **(20 points)**

Virtual page index	Physical page #	Present
0	3	Y
1	7	N
2	6	N
3	5	Y
4	14	Y
5	30	Y
6	26	Y
7	11	Y
8	13	N
9	18	N
10	10	Y
11	56	Y
12	110	Y
13	33	Y
14	12	N
15	25	Y

Virtual page accessed	TLB (hit or miss)	Page table (hit or fault)
1		
5		
9		
14		
10		
6		
15		
12		
7		
2		